

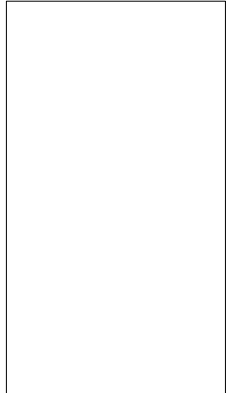


CIRRUS EDB930X ENGINEERING DEVELOPMENT BOARD

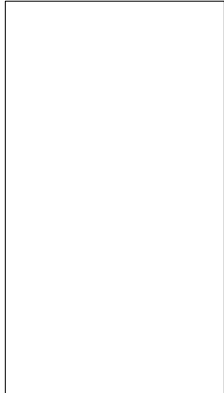
REVISION2

SHEET 1 OF 6

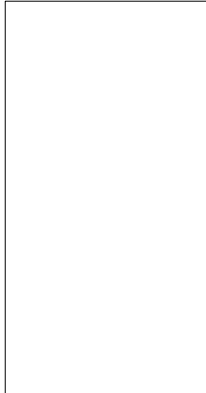
Audio
PG5_Audio.sch



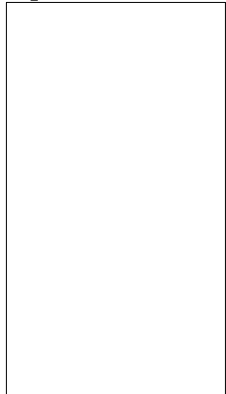
CS930X
PG2_CS930X.sch



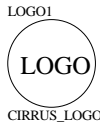
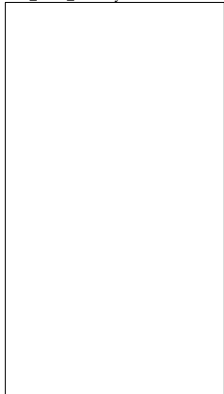
Power1
PG6_Power1.sch



Ethernet1
PG4_Ethernet1.sch

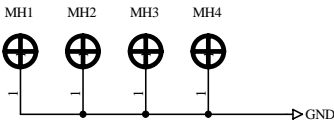
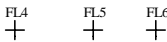


930X memory schematic
PG3_930X_Memory.SCH



GLOBAL FIDUCIALS

TOP SIDE



Notes: (unless otherwise stated)

1. All resistors are listed in ohms and are 5%, 1/10 W, Metal Film (0603 form factor)
2. All capacitors are listed in microfarads, and are 10%, 25V, Ceramic, X7R (0603 form factor)
3. All inductors are listed in microhenries, and are 5%, 100ma, non-wound (0805 form factor)
4. Signal Ports are global, and are all connected through sheet symbols
5. Signal Names are local, and apply only to the current sheet.

Sheet Index

1. TOP LEVEL SCHEMATIC
2. CS9301 CPU
3. CS9301 MEMORY SCHEMATIC
4. ETHERNET SCHEMATIC
5. AUDIO SCHEMATIC
6. POWER SCHEMATIC

ECN CHANGES FROM REV 1 TO REV 2

1. Change C53 to 47pf
2. Reverse power and ground on U8
3. Make sure all jumpers are correctly called out on the schematics the way they are to be connected on the board.
4. Remove signal SDOUT from JP12 and put signal SDIN in place.
5. Remove USB Maxim power switch and add fuse in place.
6. Correct alignment with GPIO headers.
7. Remove legend and put silkscreen at jumper location
8. Move headers for test0 and test1 over to allow for easier access. Also have test0 to outside edge of board
9. remove bottom silkscreen
10. Add correct silk for RS232 com ports for Uart1 and Uart2
11. change LED2 to red
12. place DNP 1x2 header for alternative power source.
13. On pin 14 of audio dac remove net resetn and place egpio1 net in place. Place a 1K pull down on the egpio1 line.

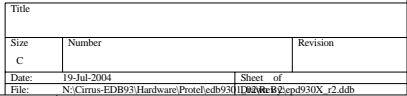
CHANGES FROM 9301 REV 2 TO 9302 BOARD PLATFORM

1. Change the part number of the 9301 to 9302
2. Change the following USB circuitry from Do not populate to populated: C109, C111, F1 C113, C115, C117, R125-128, J8

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REVISION 2

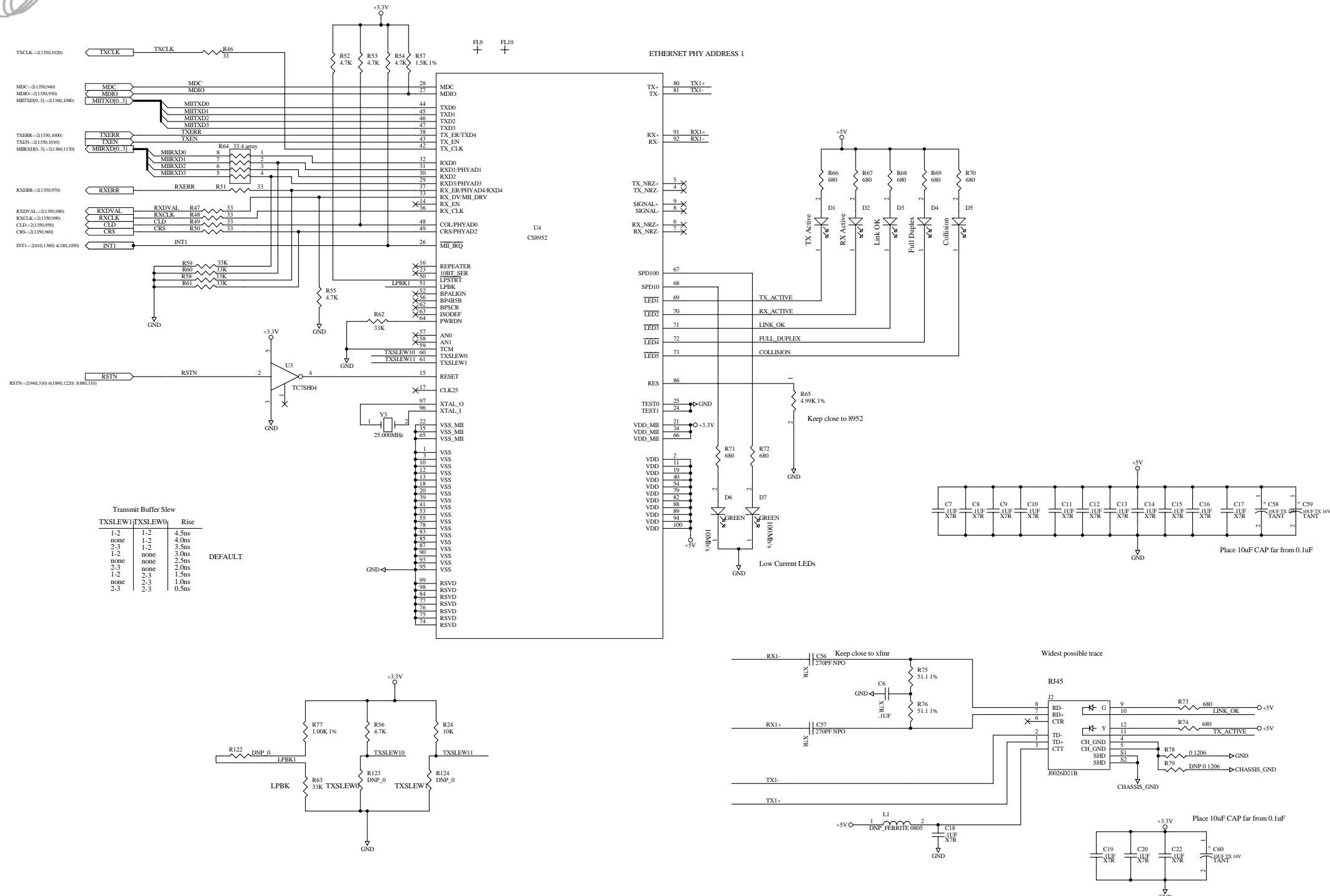




ETHERNET INTERFACE (MII Address) SCHEMATIC

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REVISION 2

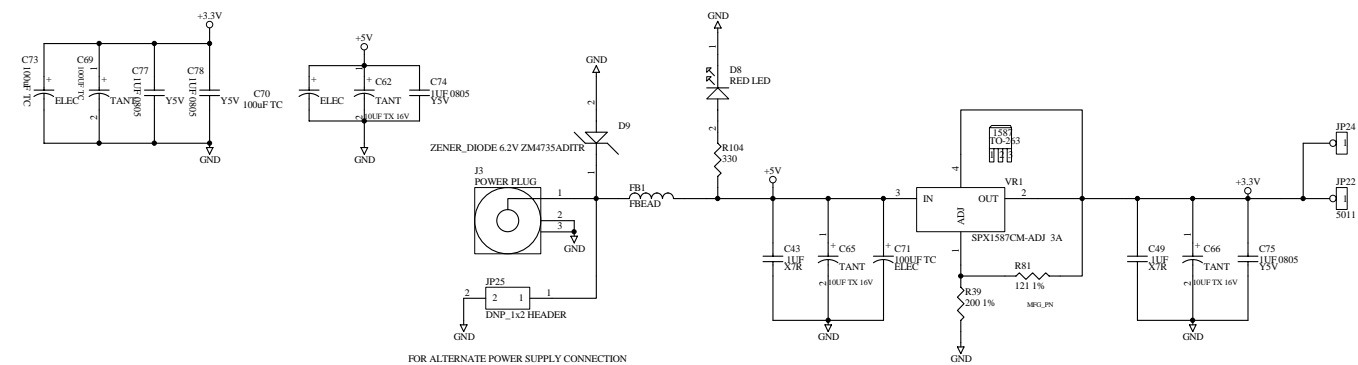
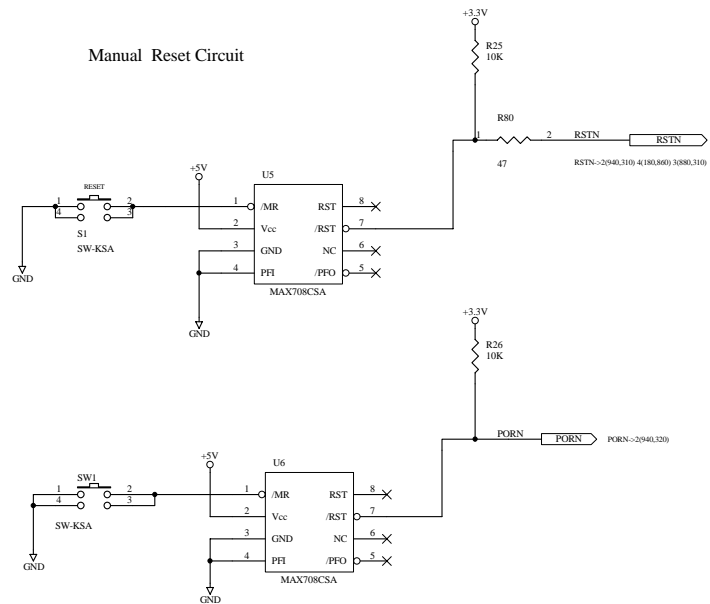
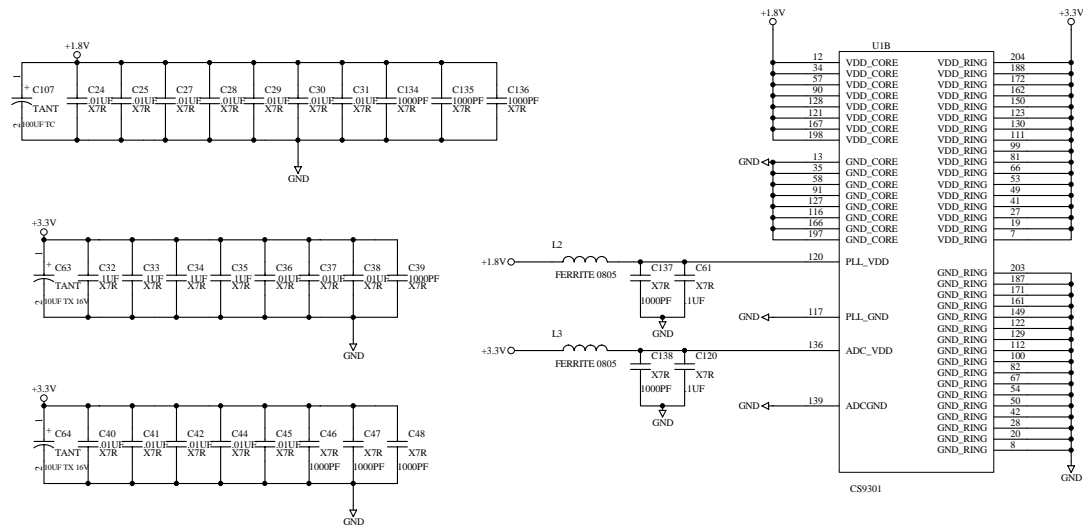




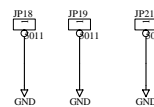
POWER SCHEMATIC

SHEET 6 OF 6

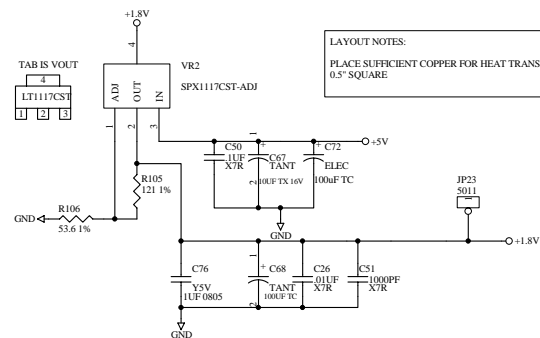
REVISION 2



GND TESTPOINTS



+1.8V REGULATION



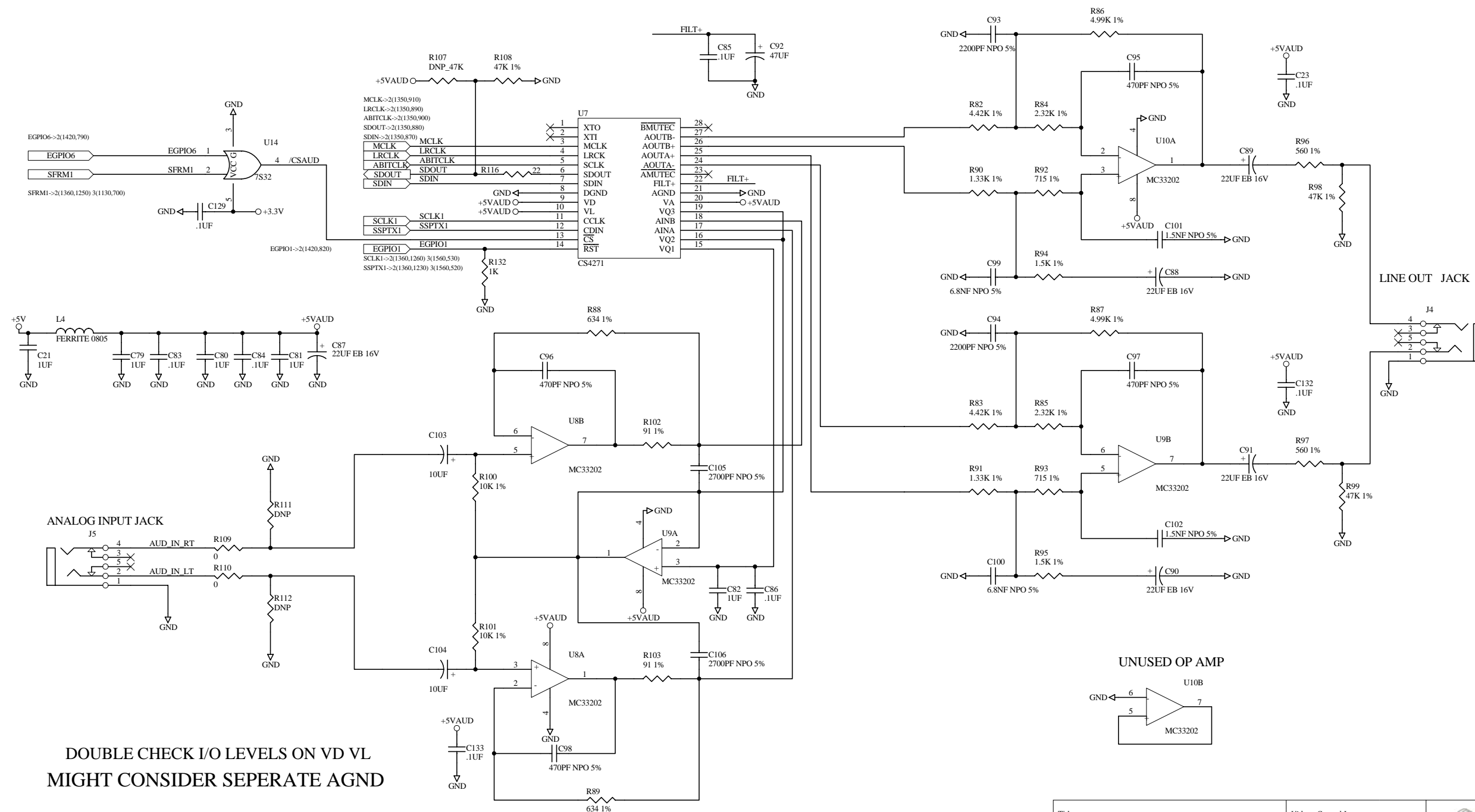
LAYOUT NOTES:
PLACE SUFFICIENT COPPER FOR HEAT TRANSFER
0.5" SQUARE

Title
POWER SCHEMATIC
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Second Floor
State College, PA 16803
Date: 19-Jul-2004

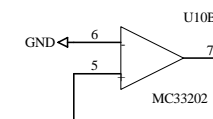



REVISION2



DOUBLE CHECK I/O LEVELS ON VD VL
MIGHT CONSIDER SEPERATE AGND

UNUSED OP AMP

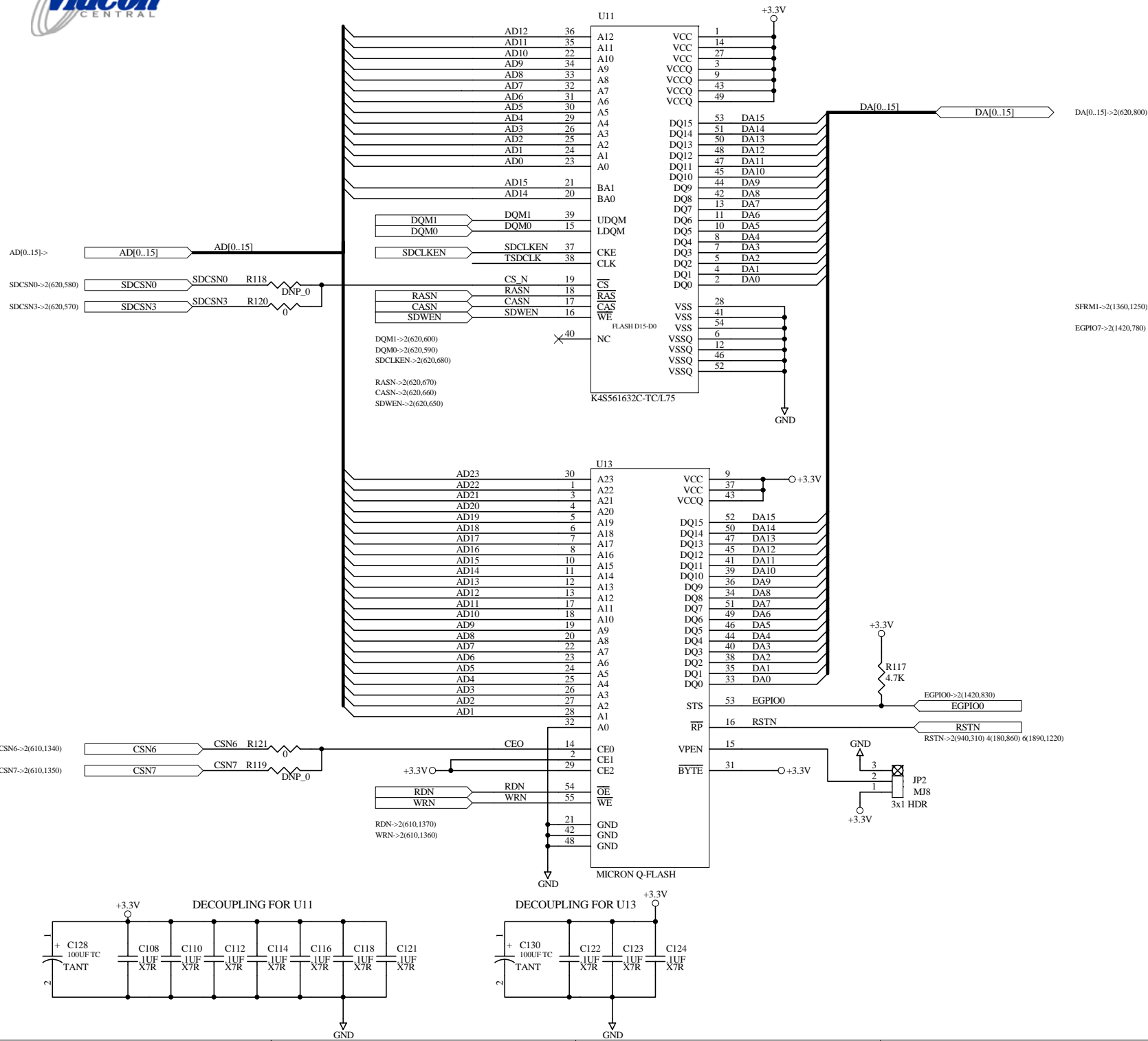


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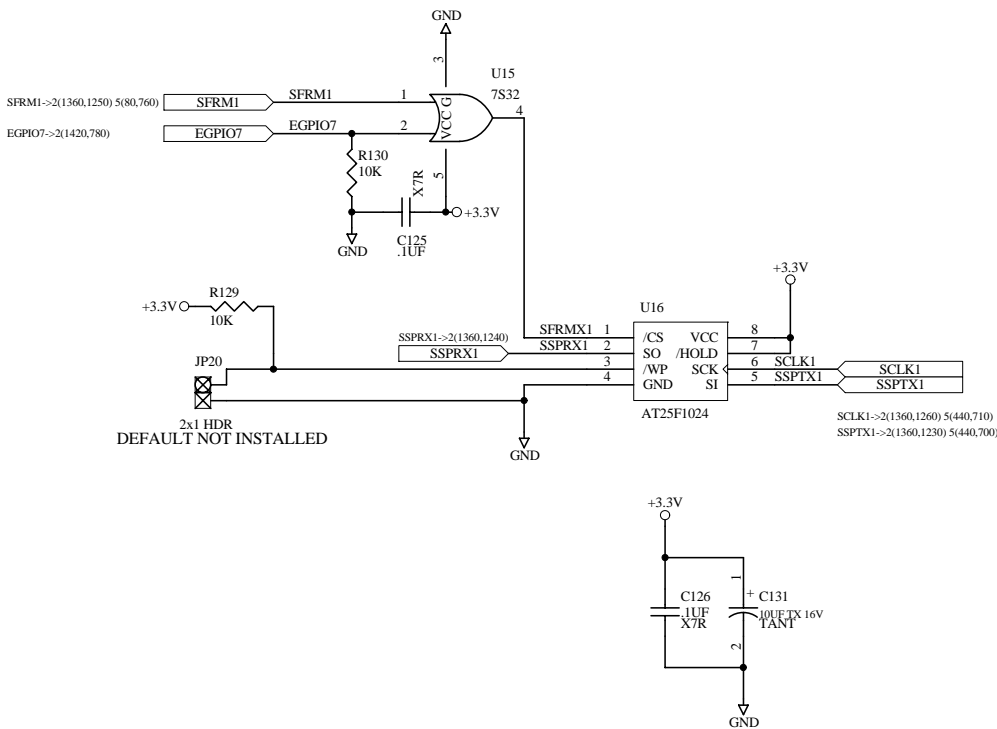
930X MEMORY & FLASH SCHEMATIC

SHEET 3 OF 6

REVISION2



EEPROM INTERFACE



董庭江 (Powerdong)
Honestar technologies Co.,Ltd Beijing Office
北高智科技有限公司北京办事处
Add: Qantum Plaza, No. 23 Zhi Chun Road, Haidian District, Beijing
北京市海淀区知春路23号量子银座408室 100083
Tel: 86-10-82358601~4 Fax: 86-10-82358605
Mobile: 13811697551
Email: power.dong@honestar.com
Website: www.honestar.com

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